Docket: 740819-734

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re National Phase Patent Application of	)
Akira ASAI et al.	)
International Application No. PCT/JP01/04344	) Attn: US/DO/EO
International Filing Date: May 23, 2001	)
For: BIPOLAR TRANSISTOR AND	)
FABRICATION METHOD THEREOF	) Date: January 22, 2002

PRELIMINARY AMENDMENT

Honorable Commissioner for Patents and Trademarks
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE CLAIMS:

Please amend claim 5 as follows: Please note that claim 5 is presented below in its amended form. It is further presented as an Attachment to the Amendment whereby the amendment to the claim is outlined using the conventional method of bracketing and underlining.

5. (Amended) The bipolar transistor according to any one of claims 1 through 3, wherein:

said substrate is a silicon substrate;

said first semiconductor layer is an Si layer;

said second semiconductor layer is an SiGe layer or an SiGeC layer; and

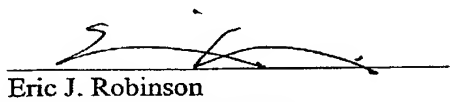
said third semiconductor layer is an Si layer.

REMARKS

Claim 5 has been amended to correct the multiple dependencies therein.

Examination on the merits is requested.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

5. (Amended) The bipolar transistor according to any one of claims 1 through [4] 3, wherein:

said substrate is a silicon substrate;

said first semiconductor layer is an Si layer;

said second semiconductor layer is an SiGe layer or an SiGeC layer; and

said third semiconductor layer is an Si layer.